1. (Currently Amended) A two terminal device comprising:
a nucleation layer;
a nitride layer on said nucleation layer; ~~and~~
a re-oxide layer on said nitride layer; and [,]
a conductor on said re-oxide layer;
wherein said nitride layer ~~and an interface between nitride layer and said re-oxide layer include~~ includes electron traps.

2. (Currently Amended) The device in claim 1, wherein characteristics of said ~~carrier~~ electron traps control a voltage output of said device.

3. (Original) The device in claim 1, wherein a thickness of said nitride layer and said re-oxide layer control a voltage output of said device.

4. (Original) The device in claim 1, wherein said nitride layer and said re-oxide layer comprise one of a voltage regulator, voltage sensor, and memory device.

5. (Original) The device in claim 1, wherein said capacitor undergoes a trap filled limit voltage, such that a constant voltage is output for a plurality of currents.

6. (Original) The device in claim 5, wherein trap filled limit voltage events occur at different voltage levels, such that said device comprises a multi value voltage regulator.

7. (Currently Amended) A capacitor voltage regulator device comprising:
a nucleation layer;
a nitride layer on said nucleation layer; ~~and~~
a re-oxide layer on said nitride layer; and [,]

a conductor on said re-oxide layer;

wherein said nitride layer ~~and an interface between nitride layer and said re-oxide layer include~~ includes electron traps, and

wherein ~~characteristics of said carrier traps~~ a thickness of said nitride layer controls ~~control~~ a voltage output of said structure.

8. (Currently Amended) The device in claim 7, wherein a thickness ~~of said nitride layer and~~ said re-oxide layer ~~control~~ controls a voltage output of said device.

9. (Original) The device in claim 7, wherein said capacitor undergoes a trap filled limit voltage, such that a constant voltage is output for a plurality of currents.

10. (Original) The device in claim 9, wherein trap filled limit voltage events occur at different voltage levels, such that said device comprises a multi value voltage regulator.

11. (Currently Amended) A method of manufacturing a capacitor structure, said method comprising:

thermally growing a ~~thermal nitride~~ nucleation layer on a ~~buried plate~~ substrate;

performing a low pressure chemical vapor deposition (LPCVD) of silicon nitride on said nucleation layer; ~~and~~

re-oxidizing a top portion of said silicon nitride to form a re-oxide layer~~, such that said nitride layer and an interface between said silicon nitride layer and said re-oxide layer include electron traps~~; and

forming a conductor on said re-oxide layer,

wherein said nitride layer includes electron traps.

12. (Original) The method in claim 1, wherein characteristics of said carrier traps control a voltage output of said device.

13. (Original) The method in claim 11, wherein a thickness of said nitride layer and said re-oxide layer modulate a voltage output of said device.

14. (Original) The method in claim 11, wherein said nitride layer and said re-oxide layer comprise one of a voltage regulator, voltage sensor, and memory device.

15. (Original) The method in claim 11, wherein said capacitor undergoes a trap filled limit voltage, such that a constant voltage is output for a plurality of currents.

16. (Original) The method in claim 15, wherein trap filled limit voltage events occur at different voltage levels, such that said capacitor device comprises a multi value voltage regulator.